REMARKS

Reconsideration of this application in light of the above amendments is courteously solicited.

Claim 1 has been amended so as to overcome the Examiner's objection raised under 35 U.S.C. 112.

Applicants submit herewith a proposed drawing correction to Figure 3 wherein the legend "Prior Art" has been added. The Examiner's approval of this drawing correction is respectfully requested.

With regard to the prior art rejection set forth by the Examiner in paragraphs 5, 6, 7 and 8 of his office action, Applicants respectfully request reconsideration for the reasons set forth hereinbelow.

The instant application currently contains two independent claims, independent claim 1 drawn to a cache memory and independent claim 6 drawn to a method for reducing a penalty occurring upon a cache miss. Applicants respectfully request the Examiner to reconsider this rejection of both of the independent claims for the reasons set forth hereinbelow.

Independent claim 1 sets forth the following:

> A cache memory for three-dimensional graphics texture mapping, comprising:
> first and second DRAM banks including SAM ports, respectively, each of said SAM ports reading a texture for a trilinear interpolation and fetching new texture

sub-clips from the outside;

a sub-clip loader connected to said SAM ports of said first and second DRAM banks and for fetching new texture sub-clips from an external memory;

a controller for controlling said components; and

a CAM for checking if eight texels existing at an integer coordinate relative to an LOD and (u, v) coordinates are located in said first and second DRAM banks, when the LOD and (u, v) coordinates mapped into a texture space with respect to a pixel to be rendered on a display screen are input to said controller.

The Examiner, in rejecting independent claim 1 asserts that Migdal et al., U.S. Patent 6,417,860, teaches all of the limitations of the above noted claim 1 with the exception of the DRAM having a SAM port. Applicants respectfully traverse the Examiner's rejection of claim 1.

The present invention applies a clipmap concept into the relation between a system memory and a texture cache. In this regard, for example, see Figure 7. The present invention provides a new cache memory capable of accelerating the texture mapping process. The 6,417,860 patent fails to teach, disclose, suggest or render obvious the clipmap concept between a system memory and a texture cache as claimed. The '860 patent teaches a method for reducing the required capacity of system memory wherein the clipmap concept is applied into the relation between a hard disk and system memory (in this regard see Figure 2) by implementing it in an entirely software manner. This is not suitable for accelerating the texture mapping. As

noted above, with respect to the present invention, a new cache memory capable of accelerating the textured mapping process is implemented in a hardware manner. Accordingly, it cannot be said that the '860 patent teaches all the limitations of claim 1 with the exception of the DRAM having an SAM port. Accordingly, it is submitted that independent claim 1 defines over the prior art.

With respect to dependent claim 4, it is submitted that dependent claim 4 contains patentable merit in its own right. Claim 4 provides a plurality of data paths for performing a trilinear interpolation in one clock cycle by accessing eight texels simultaneously. The tertiary reference to Sara applied by the Examiner teaches eight RAMs for this purpose.

With regard to dependent claim 5, again it is submitted that claim 5 contains patentable merit in its own right. The sub-clip predictor of the present invention is a prefetching controller (see Figure 8) for prefetching texture data predicted to be used at the next time in a 3-dimensional space considering movements of LOD level as well as in 2-dimensional space. The Park reference does not teach the prefetching of another texture data predicted to be used the next time in 3-dimensional space. Park teaches a prefetching controller for prefetching in 2-

dimensional space. Accordingly, it is submitted that claim 5 is patentable over the prior art.

Method claim 6 is likewise patentable over the prior art. In accordance with claim 6, the present invention discloses a method for reducing a penalty occurring upon a cache miss, the method comprising a stack layer prediction step (prediction in 3-dimensional space) as well as a sub-clip prediction step in one stack layer (prediction in 2-dimensional space). As noted above, the secondary reference to Park teaches a method for prefetching the next texture data by using the address from the address generator based on the directional signal in 2-dimensional space. Accordingly, it cannot be said that claim 6 is rendered obvious by the teachings of the Migdal et al. reference in view of Park.

In light of the foregoing it is submitted that all of the claims as pending patentably define over the art of record and an early indication of same is respectfully requested.

An earnest and thorough attempt has been made by the undersigned to resolve the outstanding issues in this case and place same in condition for allowance. If the Examiner has any questions or feels that a telephone or personal interview would be helpful in resolving any outstanding

issues which remain in this application after consideration of this amendment, the Examiner is courteously invited to telephone the undersigned and the same would be gratefully appreciated.

It is submitted that the claims as amended herein patentably define over the art relied on by the Examiner and early allowance of same is courteously solicited.

If any fees are required in connection with this case, it is respectfully requested that they be charged to Deposit Account No. 02-0184.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231

on January 28, 2003
(Date of Deposit)

Rachel Piscitelli
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Signature

January 28, 2003
Date of Signature

Respectfully submitted,

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Version with markings to show changes made to claim

1. (Amended) A cache memory for three-dimensional graphics texture mapping, comprising:

first and second DRAM banks including SAM ports, respectively, each of said [SRAM] SAM ports reading a texture for a trilinear interpolation and fetching new texture sub-clips from the outside;

a sub-clip loader connected to said SAM ports of said first and second DRAM banks and for fetching new texture sub-clips from an external memory;

a controller for controlling said components; and

a CAM for checking if eight texels existing at an integer coordinate relative to an LOD and (u, v) coordinates are located in said first and second DRAM banks, when the LOD and (u, v) coordinates mapped into a texture space with respect to a pixel to be rendered on a display screen are input to said controller.